Amendment after Final Rejection under 37 C.F.R. 1.116
Applicant: Frederick A. Perner et al.
Serial No.: 10/681,483
Filed: October 8, 2003
Docket No.: 10014200-1
Title: MEMORY WITH CONDUCTORS BETWEEN OR IN COMMUNICATION WITH STORAGE UNITS

Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory, comprising:

an array of magnetic memory cells, each magnetic memory cell having sides and opposite ends and being adapted to store a bit of information;

interconnects in communication with the magnetic memory cells; and

conductors in communication with the magnetic memory cells and the interconnects, the conductors filling spaces between adjacent magnetic memory cells of the array as viewed from the sides of the magnetic memory cells;

wherein the conductors comprise top conductors, the memory further comprising bottom conductors disposed generally orthogonally to the top conductors, each bottom conductor supporting multiple magnetic memory cells of the array;

further wherein the top conductors are deposited between the bottom conductors and between adjacent magnetic memory cells of the array.

2. (Currently Amended) The memory of claim 1, wherein the ~~conductors comprise~~ top conductors are formed by a patterning process that also patterns the magnetic memory cells.

3. (Original) The memory of claim 1, further comprising a substrate, wherein the array of magnetic memory cells is supported on the substrate and wherein the interconnects pass at least partially through the substrate.

4. (Original) The memory of claim 1, wherein at least one of the conductors is deposited on at least one of the interconnects and at least one other of the conductors is deposited on at least one of the magnetic memory cells.

5. (Cancelled)

6. (Cancelled)

7. (Original) The memory of claim 1, wherein the magnetic memory cells each comprise an active layer having a non-fixed magnetization and a reference layer having a fixed magnetization.

8. (Original) The memory of claim 1, wherein the conductors filling spaces between adjacent magnetic memory cells of the array are top conductors disposed between bottom conductors of the array and between the adjacent magnetic memory cells.

9. (Currently Amended) The memory of claim 1, wherein the ~~conductors comprise top conductors, the memory further comprising:~~ bottom conductors are in communication with the magnetic memory cells; and

a dielectric material is disposed between the top conductors and the bottom conductors.

10. (Original) The memory of claim 9, wherein the dielectric material insulates the magnetic memory cells.

11. (Original) The memory of claim 1, wherein each magnetic memory cell comprises a patterned stack; the memory further comprising a dielectric layer disposed on sides of the patterned stack.

12. (Original) The memory of claim 11, wherein the dielectric layer is disposed on sides of the conductors.

13–20. (Cancelled)

21. (Currently Amended) A memory, comprising:

means for storing information having logic states, the means for storing comprising a plurality of storage units defining intervening gaps between adjacent storage units; and

means for sensing the logic states of the means for storing;

wherein the means for sensing fills the intervening gaps of the means for storing and surrounds the plurality of storage units; further wherein the means for sensing surrounds ends and sides of the plurality of storage units in three dimensions.

22. (Original) The memory of claim 21, wherein the means for sensing comprises a plurality of top conductors and a plurality of bottom conductors extending generally orthogonally to the plurality of top conductors.

23. (Currently Amended) A memory structure, comprising:

magnetic cells deposited on first conductive layers, the magnetic cells in communication with first vias of the memory structure;

insulating layers deposited on sides of the magnetic cells and patterned edges of the first conductive layers; ~~and~~

second conductive layers deposited over the insulating layers and the magnetic cells, the second conductive layers contacting second vias of the memory structure; and

a substrate supporting the magnetic cells, wherein the first vias and the second vias are disposed through the substrate.

24. (Original) The memory structure of claim 23, wherein the second conductive layers fill gaps between adjacent magnetic cells.

25. (Original) The memory structure of claim 23, wherein multiple magnetic cells are deposited on a common first conductive layer.

26. (Original) The memory structure of claim 23, further comprising multiple conductors formed from the second conductive layers.

27. (Original) The memory structure of claim 26, wherein the multiple conductors directly contact the magnetic cells and directly overlie the second vias.

28. (Previously Presented) The memory of claim 1, wherein the conductors contact the opposite ends of the magnetic memory cells and are disposed along the sides of the magnetic memory cells.

29. (Previously Presented) The memory of claim 3, wherein the conductors contact the substrate between adjacent magnetic memory cells and said spaces are at a same elevation with respect to the substrate as the sides of the adjacent memory cells.

30. (Currently Amended) The memory of claim ~~5~~1, wherein the top conductors extend between the magnetic memory cells and along the sides of the magnetic memory cells to a level of the bottom conductors.

31. (Previously Presented) The memory of claim 11, wherein straight lines extending directly between adjacent magnetic memory cells pass through the dielectric layers and through the conductors filling the spaces between the adjacent magnetic memory cells.

32. (Cancelled)

33. (Cancelled)

34. (New) A memory, comprising:

an array of magnetic memory cells, each magnetic memory cell having sides and opposite ends and being adapted to store a bit of information;

interconnects in communication with the magnetic memory cells;

conductors in communication with the magnetic memory cells and the interconnects, the conductors filling spaces between adjacent magnetic memory cells of the array as viewed from the sides of the magnetic memory cells; and

a substrate, wherein the array of magnetic memory cells is supported on the substrate and wherein the interconnects pass at least partially through the substrate;

further wherein the conductors contact the substrate between adjacent magnetic memory cells and said spaces are at a same elevation with respect to the substrate as the sides of the adjacent memory cells.

35. (New) A memory, comprising:

an array of magnetic memory cells, each magnetic memory cell having sides and opposite ends and being adapted to store a bit of information;

interconnects in communication with the magnetic memory cells; and

conductors in communication with the magnetic memory cells and the interconnects, the conductors filling spaces between adjacent magnetic memory cells of the array as viewed from the sides of the magnetic memory cells;

wherein the conductors comprise top conductors, the memory further comprising bottom conductors disposed generally orthogonally to the top conductors, each bottom conductor supporting multiple magnetic memory cells of the array;

further wherein the top conductors extend between the magnetic memory cells and along the sides of the magnetic memory cells to a level of the bottom conductors.

36. (New) A memory, comprising:

an array of magnetic memory cells, each magnetic memory cell having sides and opposite ends and being adapted to store a bit of information;

interconnects in communication with the magnetic memory cells; and

conductors in communication with the magnetic memory cells and the interconnects, the conductors filling spaces between adjacent magnetic memory cells of the array as viewed from the sides of the magnetic memory cells;

wherein each magnetic memory cell comprises a patterned stack; the memory further comprising a dielectric layer disposed on sides of the patterned stack;

further wherein straight lines extending directly between adjacent magnetic memory cells pass through the dielectric layers and through the conductors filling the spaces between the adjacent magnetic memory cells.

37. (New) A memory structure, comprising:

magnetic cells deposited on first conductive layers, the magnetic cells in communication with first vias of the memory structure;

insulating layers deposited on sides of the magnetic cells and patterned edges of the first conductive layers; and

second conductive layers deposited over the insulating layers and the magnetic cells, the second conductive layers contacting second vias of the memory structure;

wherein the second conductive layers fill gaps between adjacent magnetic cells.